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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/088,086	03/21/2002	Shouichi Fuji	221109US2PCT	7109

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EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/088,086	FUJI ET AL.	
	Examiner	Art Unit	
	Luan Thai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *12-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/21/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of group I, claims 1-11 and 16, in Paper No. 5 filed 02/06/04 is acknowledged. The traversal is on the ground(s) that the search of the elected product claims would also include the classes and subclasses appropriate for searching the process claims. This is not found persuasive because these inventions are distinct for the reasons as previous mentioned on Election/Restriction paper dated 01/06/04 and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper. Furthermore, the examiner respectfully submits that searching/examining the Group II method invention in addition to the elected Group I device invention would, in fact, be more than a slight added burden.

The requirement is still deemed proper and is therefore made FINAL.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The Information disclosure Statement filed on 03/21/02 has been considered.

Drawings

4. Figures 18a, 18b and 19-21 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims **5 and 9** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim **5**, the recitation "*in a direction closer to the former direction in a reflow soldering step*" is unclear as to which the former direction is.

In claim **9**, the recitations "*a land closer to the printed wiring board*" and "*the land closer to an end of the corner portion of the grid array LSI chip*" from which the limitations "a land" and "the land" have no antecedent basis and are unclear as to whether they imply the land of the LSI chip or the land being connected to the wire of the printed wiring board.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 2, 6, 7, 10 and 16, are rejected under 35 U.S.C. 103(a) as being unpatentable over Howell (5,815,374) in combination with Jonaidi (6,091,155).

Regarding claims 1, 2, 7, 10 and 16, Howell discloses (see specifically figures 9-13) a grid array electronic component in which a grid array LSI chip (66) having a large number of lands (68) connected to a large number of lands (52) through connecting means (70), wherein the lands (52) are connected to a wire pattern (62) of a printed wiring board (50). Howell, however, does not explicitly disclose the land comprising an auxiliary land being formed at a connection portion of the land connecting a wiring pattern at a portion where an excessive tensile stress to be applied between the lands on the printed wiring board corresponding to the grid array LSI chip and the wiring pattern as the wire.

Jonaidi while related to a similar grid array electronic component design teach (see specifically figures 2-5 and 7 attached) the conventional land-wire structure as shown in Figs. 1A-1B has been modified to have the land-wire structures, as shown in Figs. 2-5, which comprise a land (38') having an auxiliary land (38") being formed at a connection portion of the land connecting a wiring pattern (40) at a portion where an excessive tensile stress is applied in a

producing step between a land (38') on the printed wiring board corresponding to the grid array LSI chip and the wiring pattern (40), which is taken outward to be connected to a via hole (36) as the wire, for the purpose of reducing the stress on the solder connection (54) between the connection means (56) and the land (38) (see Figs. 2 and 7, Col. 8, lines 44+). Jonaidi further discloses that a connection cross section area from the land (38') of the printed wiring board corresponding to the portion of the land of the grid array chip to the wiring pattern (40) is gradually varied (see Figs. 2 and 4), and the auxiliary land is formed at a connection portion around a through hole (36) connected to the wiring pattern (40) (see Fig. 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the land-wire structure having an auxiliary land being formed at a connection portion of the land connecting a wiring pattern at a portion where an excessive tensile stress, as taught by Jonaidi, to the grid array electronic component of Howell, in order to reduce the stress on the solder connection between the connection means and the land, and such application is held to be within the ordinary designing ability expected of a person skilled in the art.

Regarding claim 6, although the proposed electronic component of Howell and Jonaidi does not explicitly disclose a correcting step to correct warpage and distortion of the printed wiring board or an assembly step, as claimed, this limitation is taken to be a product by process limitation, and it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art

discloses a product, which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

9. Claims 1-11 and 16, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherman (5,784,262) in combination with Jonaidi (6,091,155).

Regarding claims 1-5, 7-8, 10-11 and 16, Sherman discloses (see specifically figures 1-7) a grid array electronic component in which a grid array LSI chip (12) having a large number of lands (14) connected to a large number of lands (18) through connecting means (16), wherein the lands (18) are connected to a wire pattern (27) of a printed wiring board (20), and wherein the wire pattern (27) connected to the land (18) has a direction corresponding to a corner portion of the grid array LSI chip (12) in the printed wiring board (see Fig. 3),

corresponding to an end of the LSI chip (12) in the printed wiring board (see Fig. 7), or corresponding to which a warpage of the printed wiring board is generated in a reflow soldering step (e.g., downwardly by its own weight) (see Figs. 5 and 7), wherein the land (52) has a different shape in corresponding to the land (68) of the corner portion of the grid array LSI chip. Sherman, however, does not explicitly disclose the land comprising an auxiliary land being formed at a connection portion of the land connecting a wiring pattern at a portion where an excessive tensile stress to be applied between the lands on the printed wiring board corresponding to the grid array LSI chip and the wiring pattern as the wire.

Jonaidi while related to a similar grid array electronic component design teach (see specifically figures 2-5 and 7 attached) the conventional land-wire structure as shown in Figs. 1A-1B has been modified to have the land-wire structures, as shown in Figs. 2-5, which comprise a land (38') having an auxiliary land (38") being formed at a connection portion of the land connecting a wiring pattern (40) at a portion where an excessive tensile stress is applied in a producing step between a land (38') on the printed wiring board corresponding to the grid array LSI chip and the wiring pattern (40), which is taken outward to be connected to a via hole (36) as the wire, for the purpose of reducing the stress on the solder connection (54) between the connection means (56) and the land (38) (see Figs. 2 and 7, Col. 8, lines 44+). Jonaidi further discloses a connection cross section area from the land (38') of the printed wiring board corresponding to the portion of the land of the grid array chip to the wiring pattern (40) being gradually

varied (see Figs. 2 and 4), the auxiliary land being formed at a connection portion around a through hole (36) connected to the wiring pattern (40) (see Fig. 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the land-wire structure having an auxiliary land being formed at a connection portion of the land connecting a wiring pattern at a portion where an excessive tensile stress, as taught by Jonaidi, to the grid array electronic component of Sherman, in order to reduce the stress on the solder connection between the connection means and the land, and such application is held to be within the ordinary designing ability expected of a person skilled in the art.

Regarding claim 6, although the proposed electronic component of Sherman and Jonaidi does not explicitly disclose a correcting step to correct warpage and distortion of the printed wiring board or an assembly step, as claimed, this limitation is taken to be a product by process limitation, and it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product, which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all

of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding claim 9, the Examiner assumes that the land/auxiliary land/wiring pattern in the proposed component of Sherman and Jonaidi is positioned at the direction toward to the corner of the LSI chip, as shown in Sherman's Figure 3; thus, the auxiliary land (38"), which connects the land (38') and the wiring pattern (34), as shown in Jonaidi's Figure 2, reads on the limitation as claimed in claim 9.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:45 AM - 4:15 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luan Thai
March 12, 2004